We claim:

1. An improved interface system for synchronous hierarchy telecommunication networks comprising a high frequency backpanel function, said system comprising

at least a central board (CM, CB1, CB2); and

one or more input/output peripheral boards (PD) for exchanging data frames (TRM1, TRM2, TRU1, TRU2) and control bytes (A1, A2, SY, H4, L),

wherein said data frames (TRM1, TRM2, TRU1, TRU2) contain said control bytes (A1, A2, SY, H4, L); and wherein said data frames (TRM1, TRM2, TRU1, TRU2) are bitwise converted before being exchanged between the peripheral boards (PD) and the central board (CM, CB1, CB2).

2. An interface system according to claim 1, wherein the central board (CM, CB1, CB2) comprises a local clock (OL1, OL2).

3. An interface system according to claim 2, wherein said control bytes (A1, A2, SY, H4, L) comprise bytes for frame alignment (A1, A2).

4. An interface system according to claim 2, wherein said control bytes (A1, A2, SY, H4, L) comprise synchronism bytes (SY, H4).

5. An interface system according to claim 2, wherein said control bytes (A1, A2, SY, H4, L) comprise bytes for monitoring the connection and switching of the active board (L).

6. An interface system according to claim 1, wherein it provides further signalling bytes (TP, HP, LP) inserted in the various

layers of said frames (TRM1, TRM2) for implementing a mapping function of the frames (TRM1, TRM2) and in band signalling.

7. An interface system according to claim 1, wherein the switch matrix (CM) comprises at least two central boards (CB1, CB2), whose local clocks (OL1, OL2) are made interdependent through the exchange of time information (IT).

8. An interface system according to claim 7, wherein said time information (IT) contains the frequency of clock signals (CKR1 ,CKR2) of the local clocks (OL1, OL2), information about frame alignment (SY), and information about multiframe synchronism (H4).

9. An interface system according to claim 7, wherein the peripheral boards (PD) comprise memory means (MSA, OCNT) for compensating jitter or wander effects on the frame alignment.

10. An interface system according to claim 7, wherein said memory means (MS; OCNT) and said time information (IT) cooperate for implementing a hitless traffic protection.